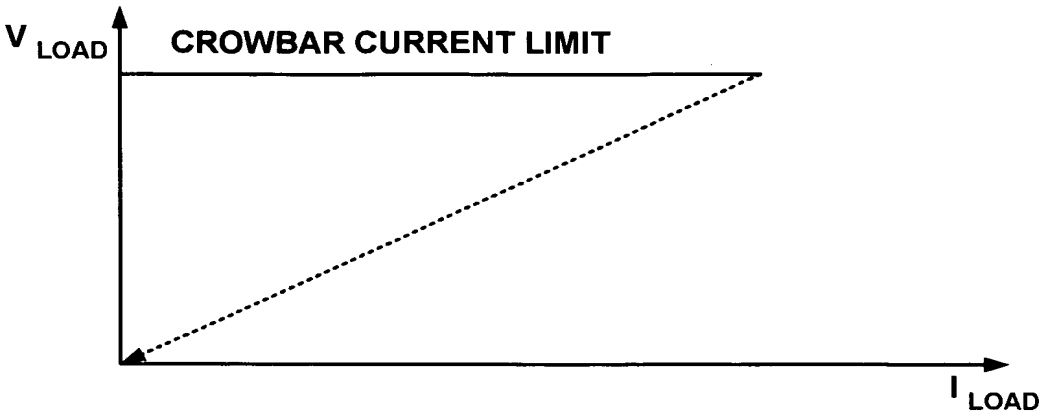

FIGURE 1A
(PRIOR ART)

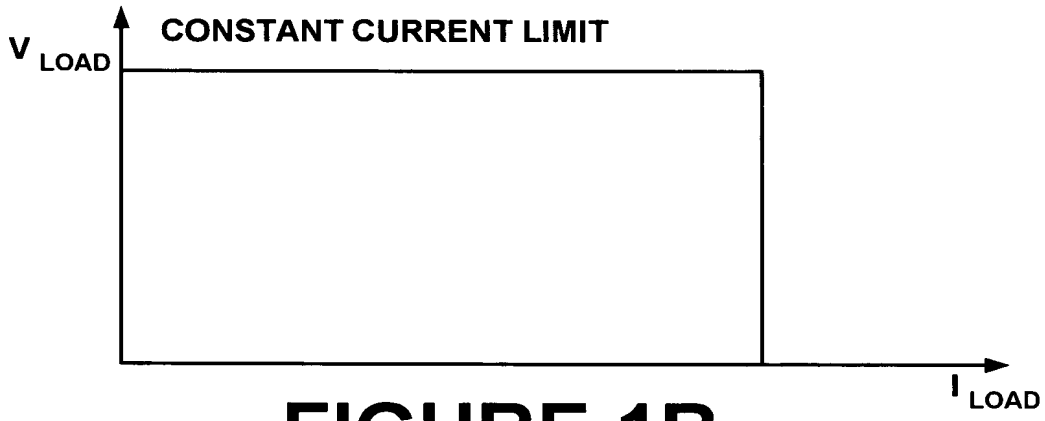

FIGURE 1B
(PRIOR ART)

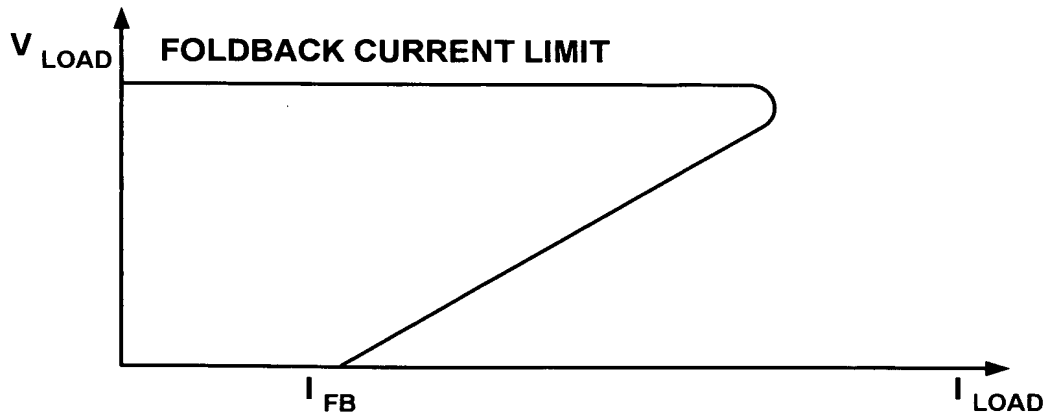

FIGURE 1C
(PRIOR ART)

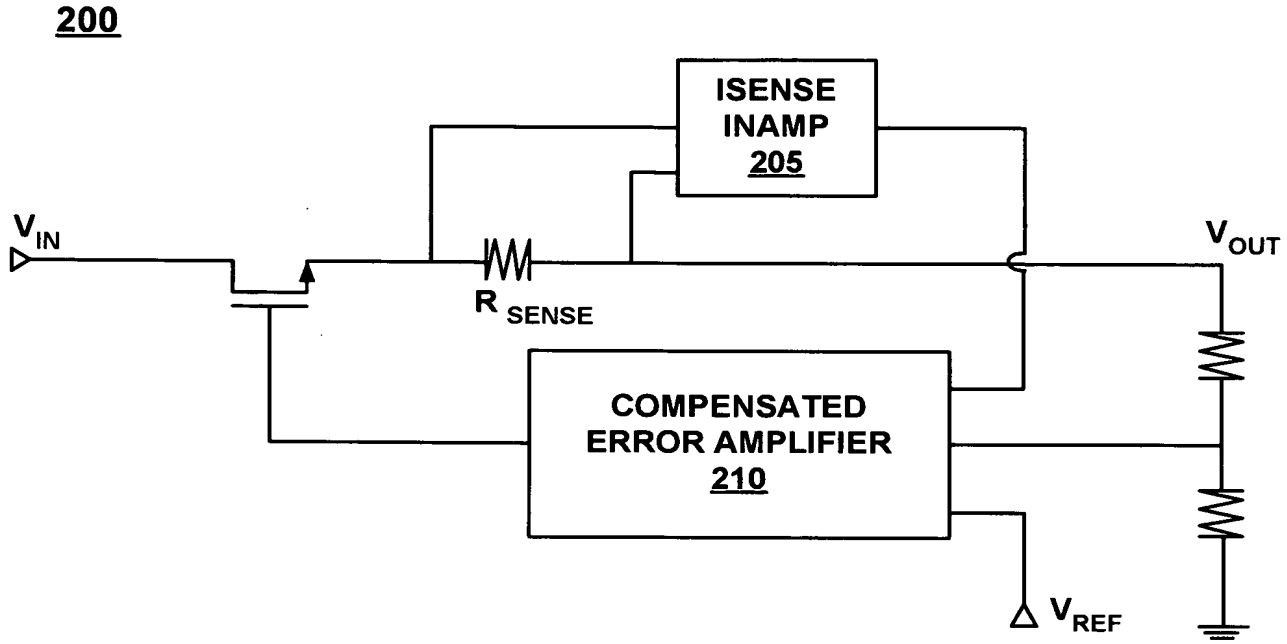

FIGURE 2A
(PRIOR ART)

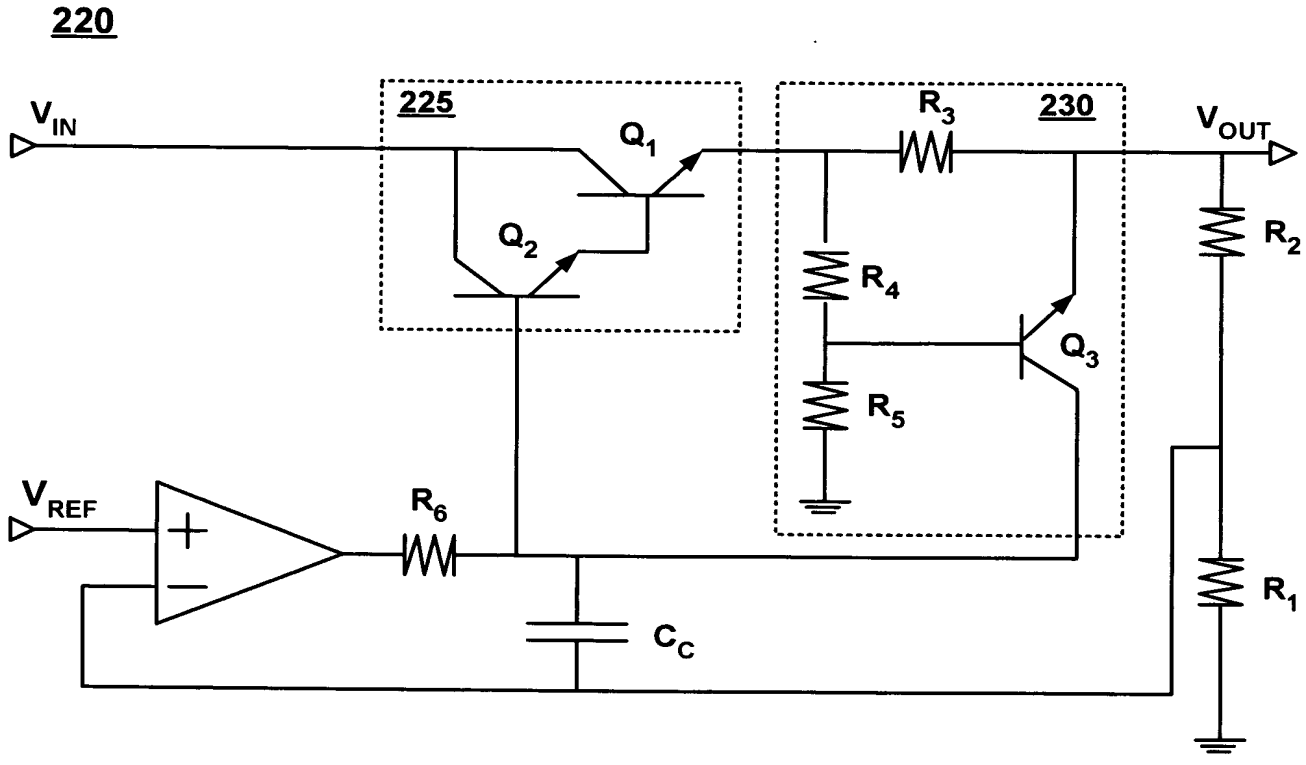

FIGURE 2B
(PRIOR ART)

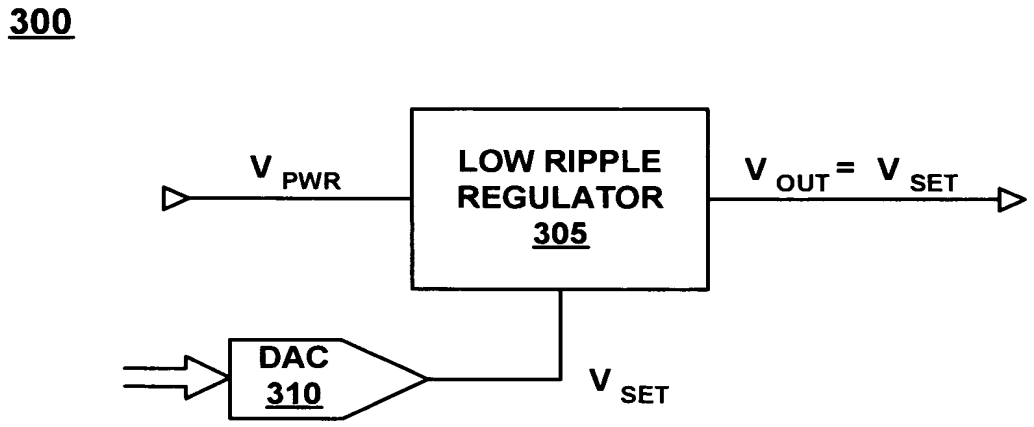

FIGURE 3A
(PRIOR ART)

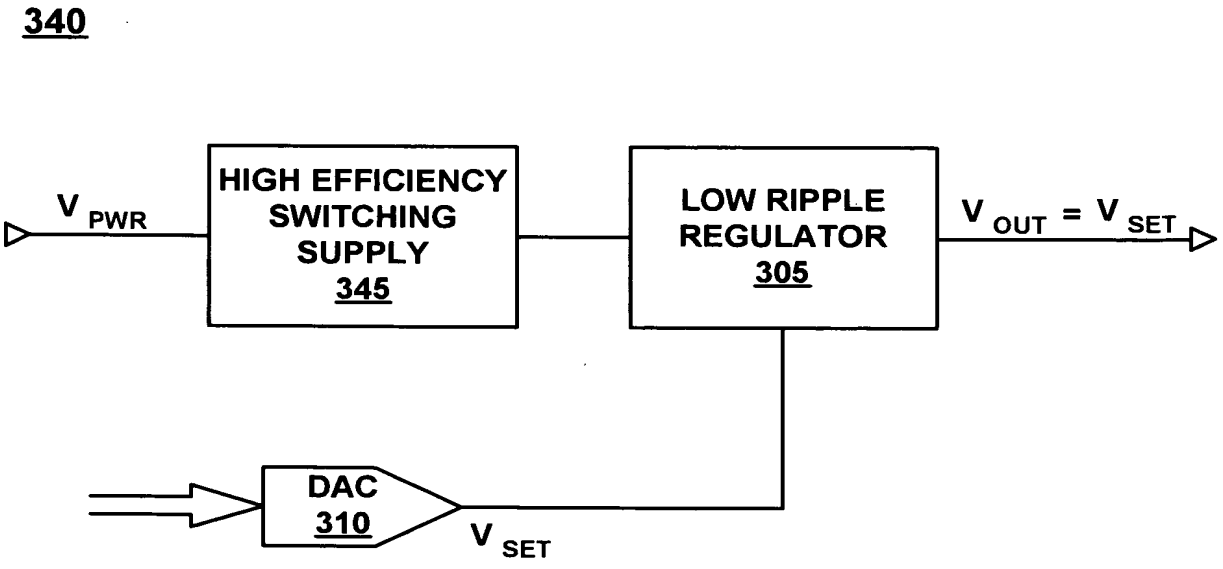

FIGURE 3B
(PRIOR ART)

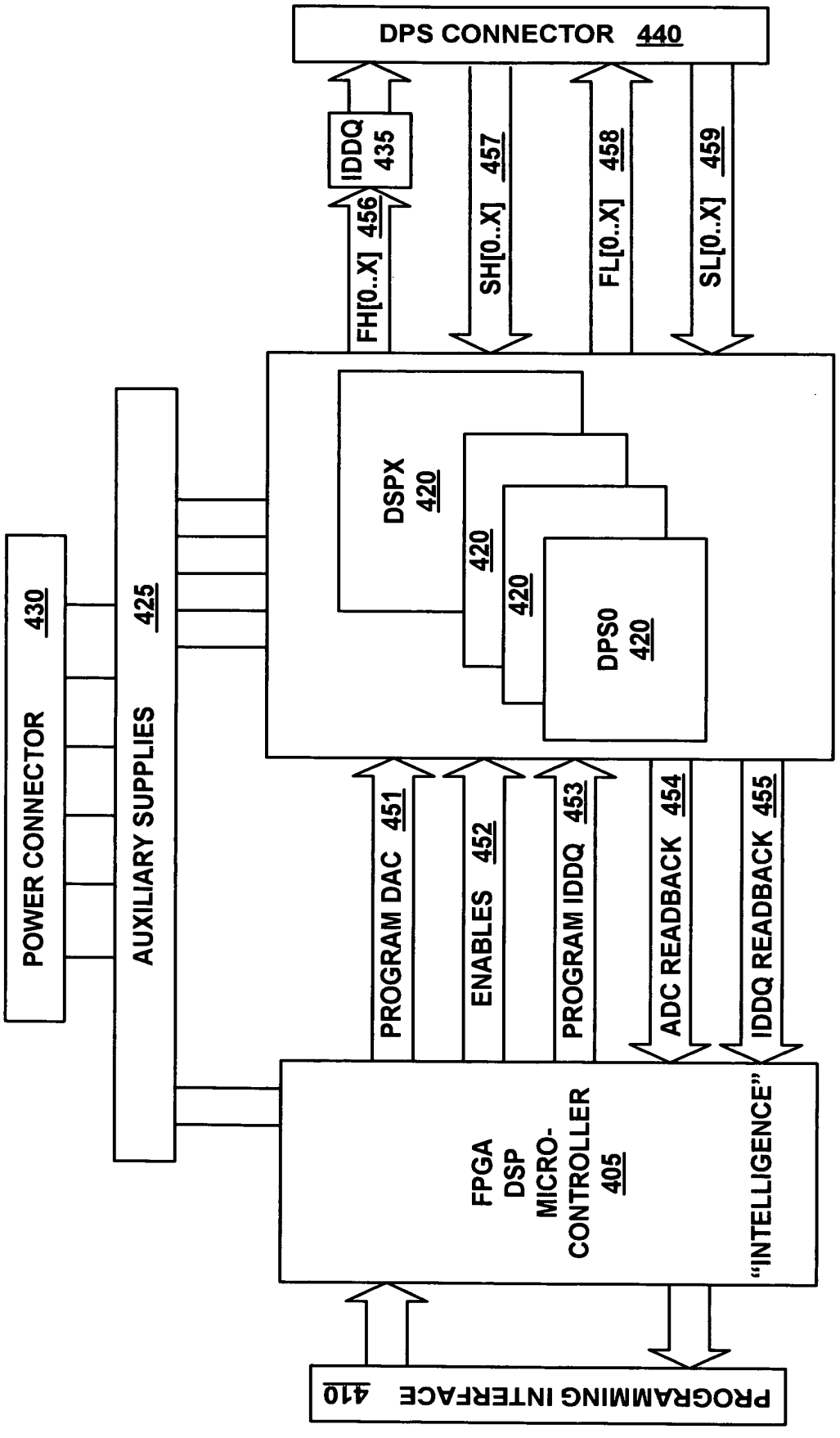
400
PROGRAMMING INTERFACE 410
FPGA DSP MICRO-CONTROLLER 405
"INTELLIGENCE"
PROGRAM DAC 451
ENABLES 452
PROGRAM IDDQ 453
ADC READBACK 454
IDDQ READBACK 455
FH[0..X] 456
SH[0..X] 457
FL[0..X] 458
SL[0..X] 459
IDDQ 435
DPS CONNECTOR 440
DSPX 420
420
420
DPS0 420
AUXILIARY SUPPLIES 425
POWER CONNECTOR 430

FIGURE 4

500

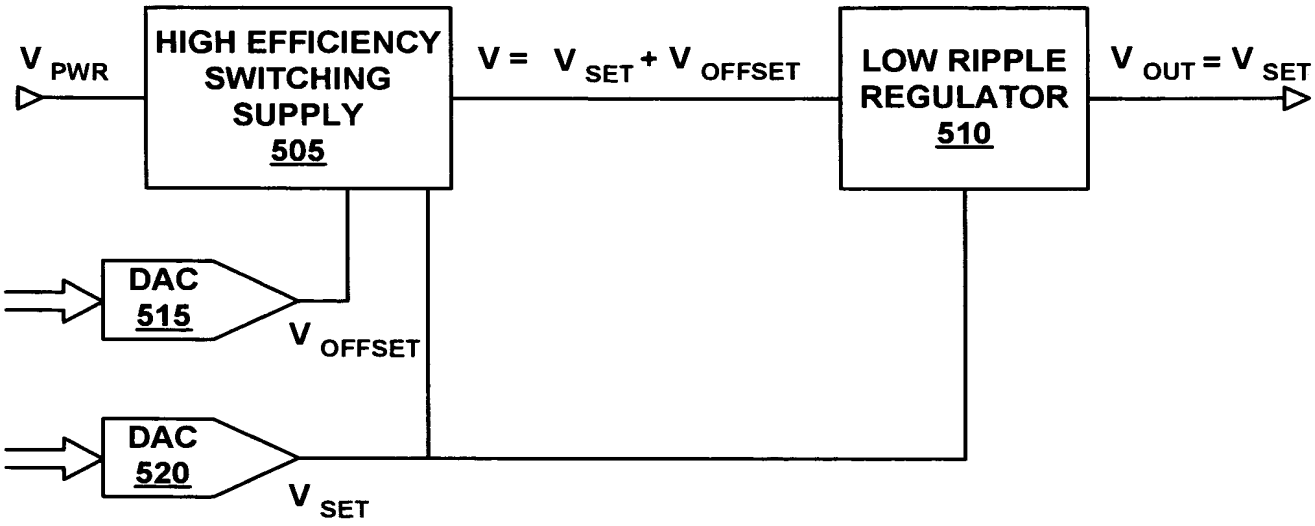
V PWR
HIGH EFFICIENCY SWITCHING SUPPLY
505
V = V SET + V OFFSET
LOW RIPPLE REGULATOR
510
V OUT = V SET
DAC
515
V OFFSET
DAC
520
V SET

FIGURE 5

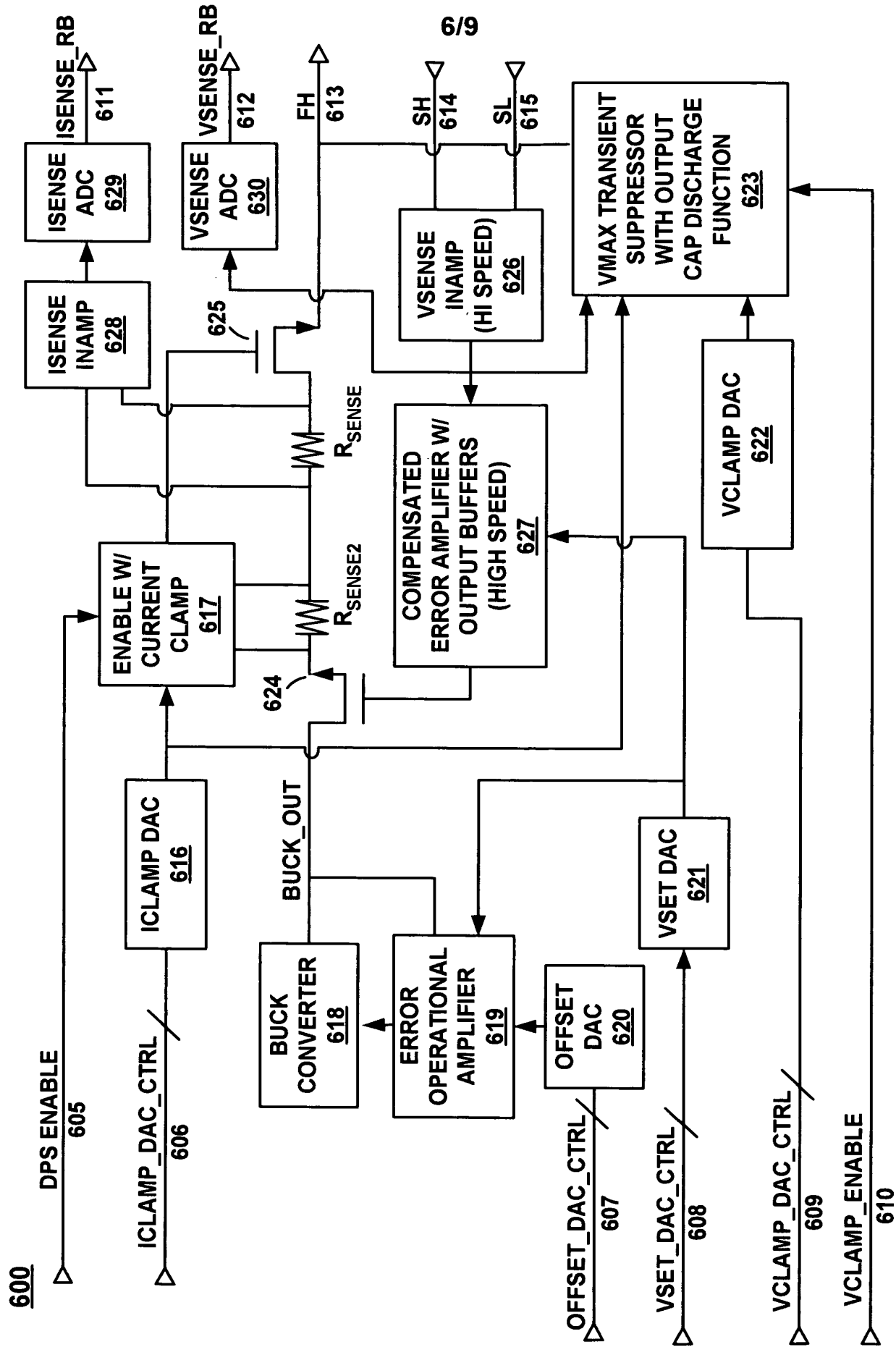
600
DPS ENABLE 605
ICLAMP_DAC_CTRL 606
OFFSET_DAC_CTRL 607
VSET_DAC_CTRL 608
VCLAMP_DAC_CTRL 609
VCLAMP_ENABLE 610
ISENSE_RB 611
VSENSE_RB 612
FH 613
SH 614
SL 615
ICLAMP DAC 616
ENABLE W/ CURRENT CLAMP 617
BUCK CONVERTER 618
ERROR OPERATIONAL AMPLIFIER 619
OFFSET DAC 620
VSET DAC 621
VCLAMP DAC 622
VMAX TRANSIENT SUPPRESSOR WITH OUTPUT CAP DISCHARGE FUNCTION 623
624
625
R_{SENSE2}
R_{SENSE}
BUCK_OUT
ISENSE ADC 629
VSENSE ADC 630
ISENSE INAMP 628
VSENSE INAMP (HI SPEED) 626
COMPENSATED ERROR AMPLIFIER W/ OUTPUT BUFFERS (HIGH SPEED) 627

FIGURE 6

700

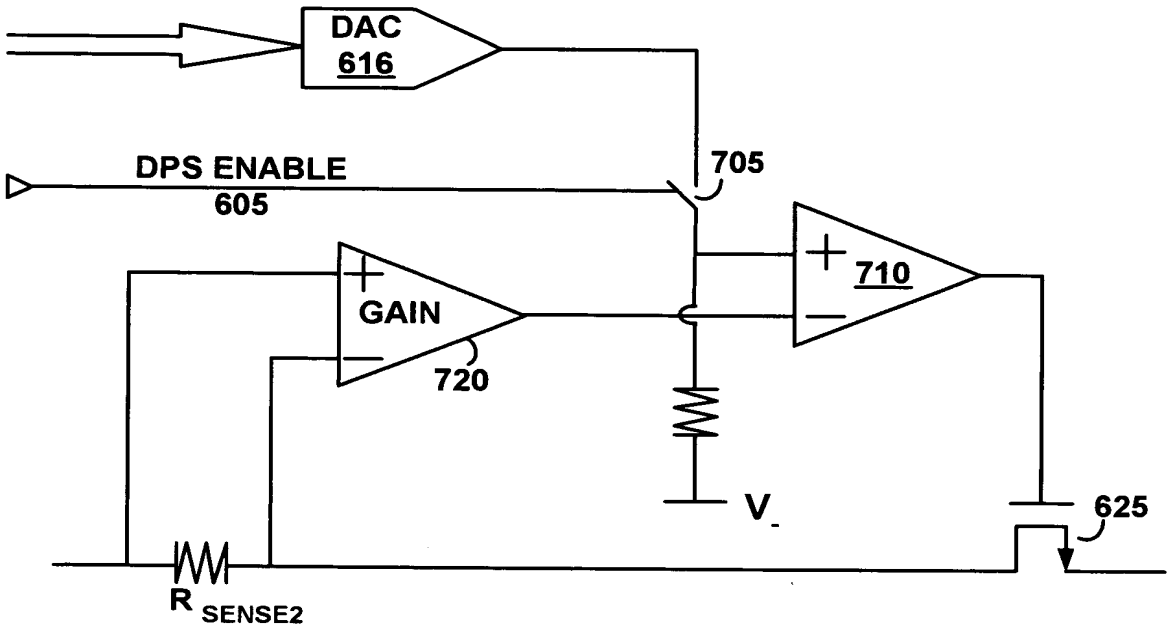

FIGURE 7

800

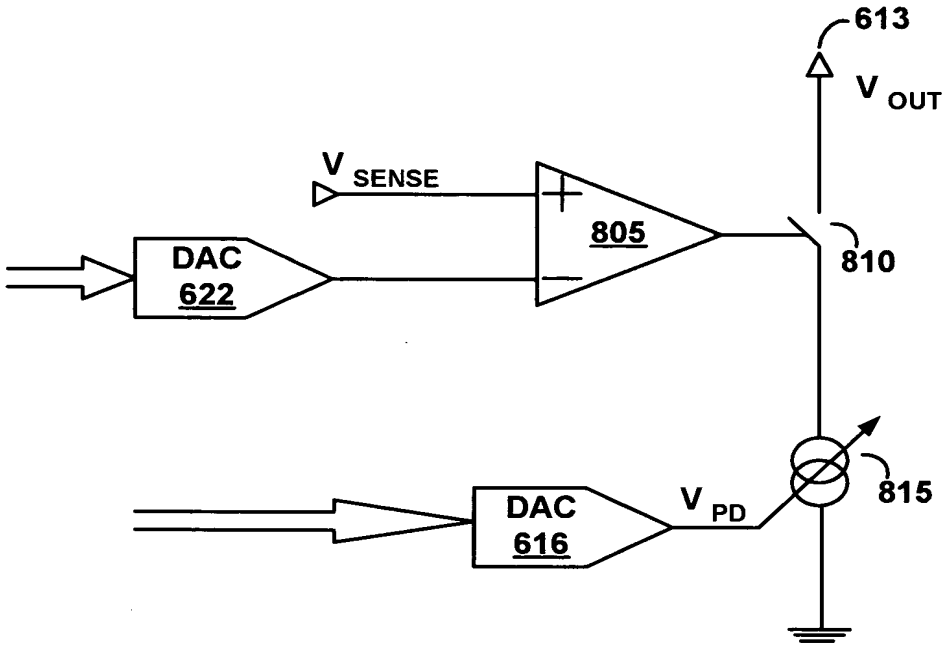

FIGURE 8

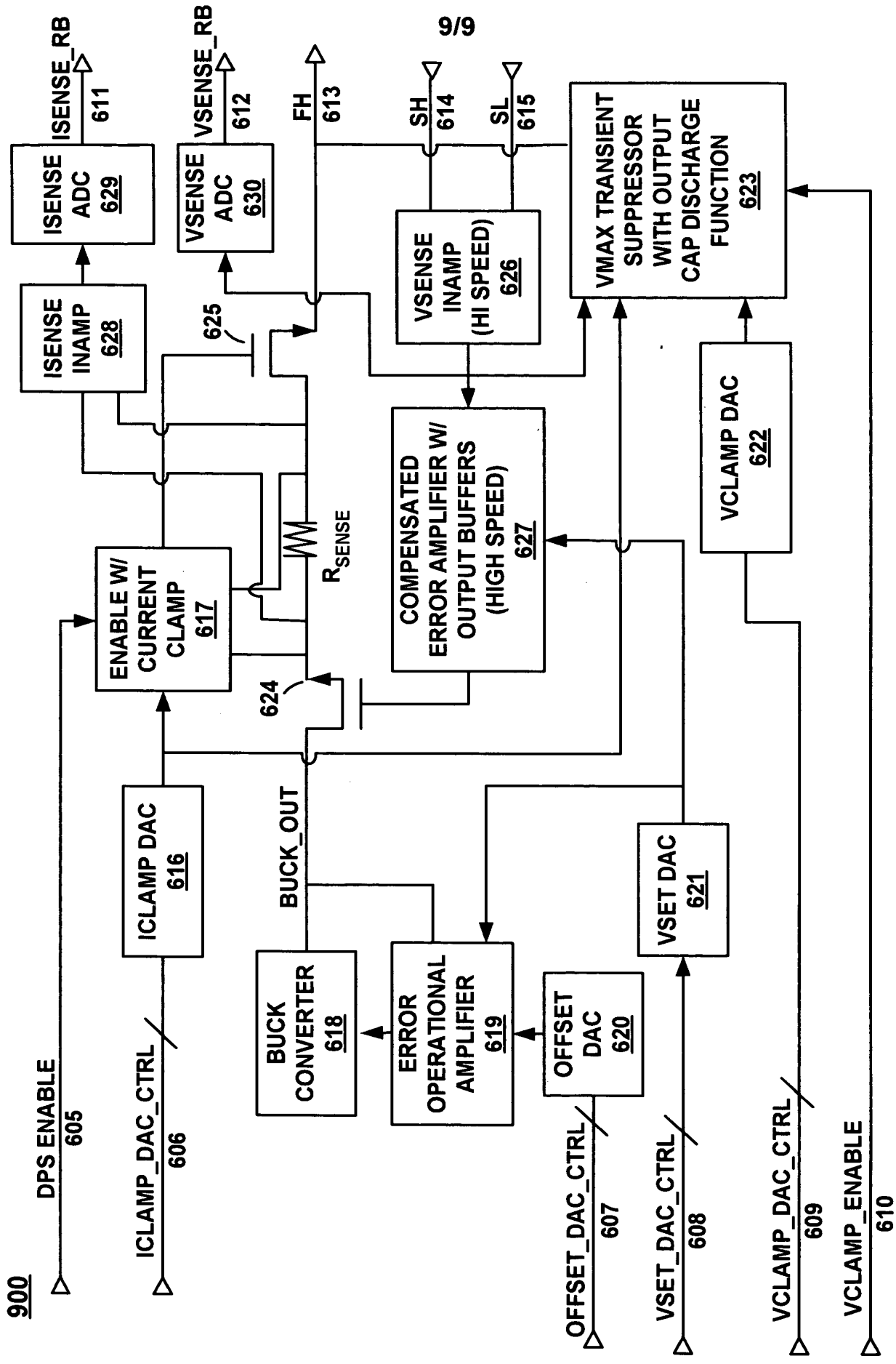
900
DPS ENABLE
605
ICLAMP_DAC_CTRL
606
OFFSET_DAC_CTRL
607
VSET_DAC_CTRL
608
VCLAMP_DAC_CTRL
609
VCLAMP_ENABLE
610
ISENSE_RB
611
VSENSE_RB
612
FH
613
SH
614
SL
615
ISENSE ADC 629
VSENSE ADC 630
ISENSE INAMP 628
VSENSE INAMP (HI SPEED) 626
VMAX TRANSIENT SUPPRESSOR WITH OUTPUT CAP DISCHARGE FUNCTION 623
625
VCLAMP DAC 622
COMPENSATED ERROR AMPLIFIER W/ OUTPUT BUFFERS (HIGH SPEED) 627
R_{SENSE}
ENABLE W/ CURRENT CLAMP 617
624
ICLAMP DAC 616
BUCK_OUT
VSET DAC 621
BUCK CONVERTER 618
ERROR OPERATIONAL AMPLIFIER 619
OFFSET DAC 620

FIGURE 9